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Fraunhofer Institute for Integrated Systems and Device Technology IISB

Examples and Future Perspectives for the Application of TCAD

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Contents

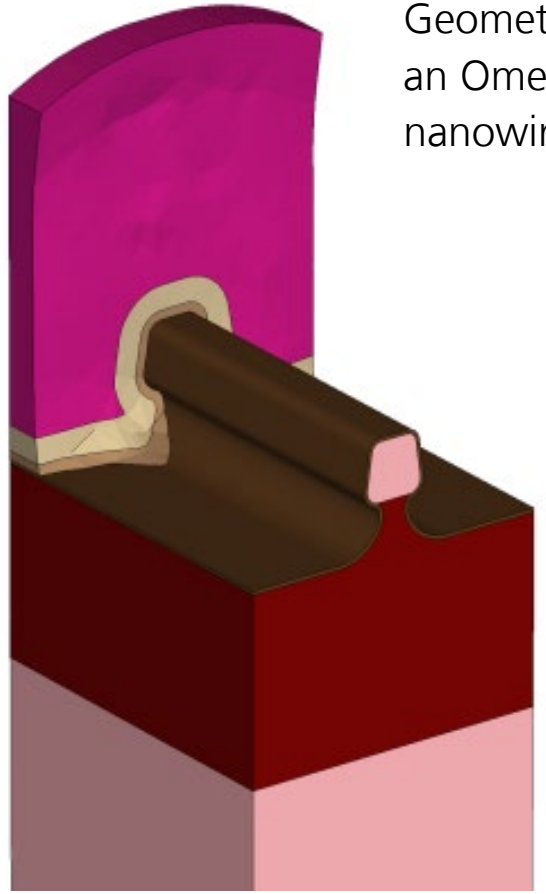
What is Technology Computer-aided Design (TCAD)?

- Process and device simulation is used in combination to study different process sequences and to investigate effects of the manufacturing process, e.g., resulting from equipment effects

- The results of process simulation are the devices (transistors, diodes, passive components, …), given by their:
  - Geometry
  - Doping distribution
  - Spatial distributions of further quantities such as mechanical stress

- These results are fed into device simulation
  - to predict the electrical behavior of the devices
  - to investigate the impact of the processing

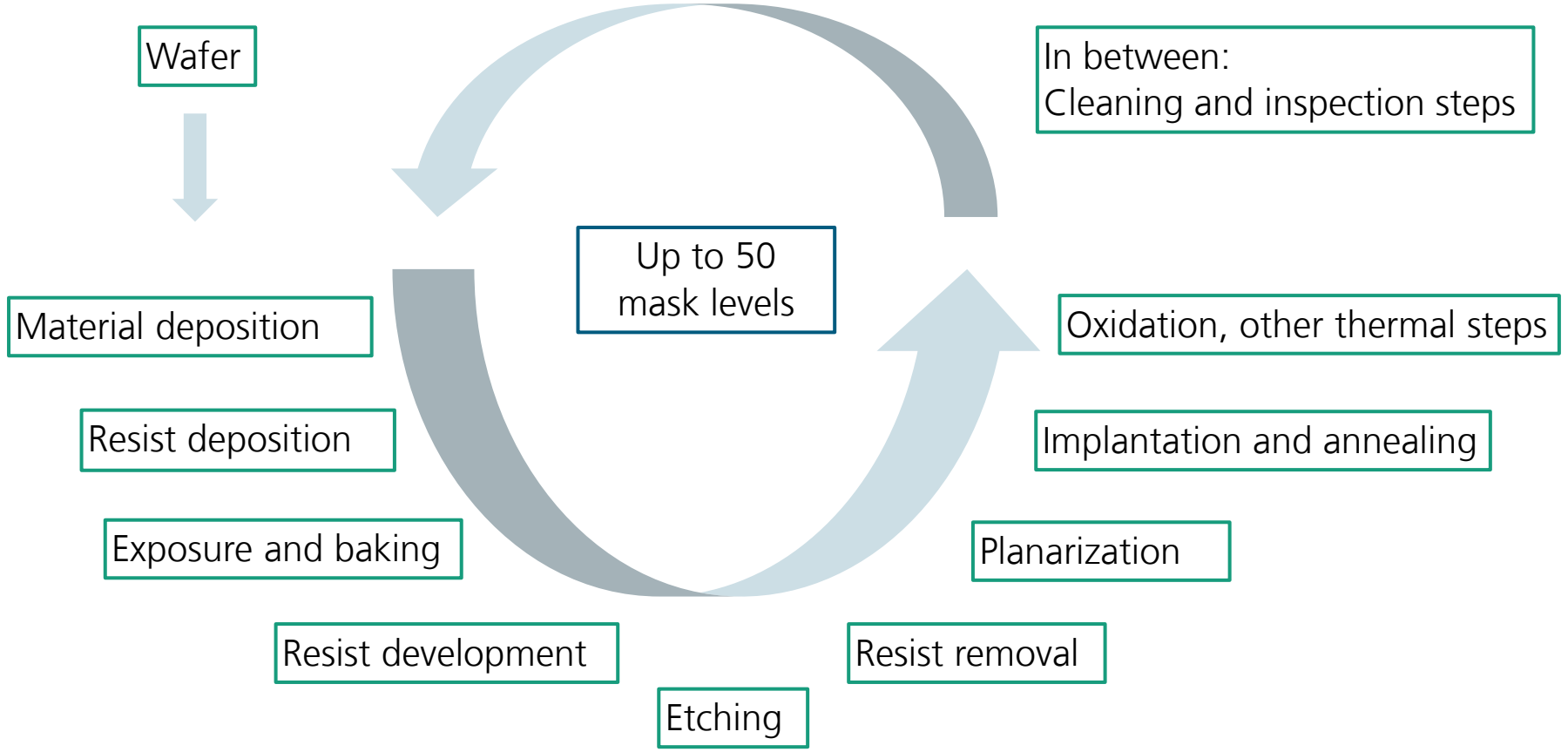
- Using this methodology, the process can be tuned in order to achieve the desired device behavior



Geometry of an Omega-gate nanowire transistor

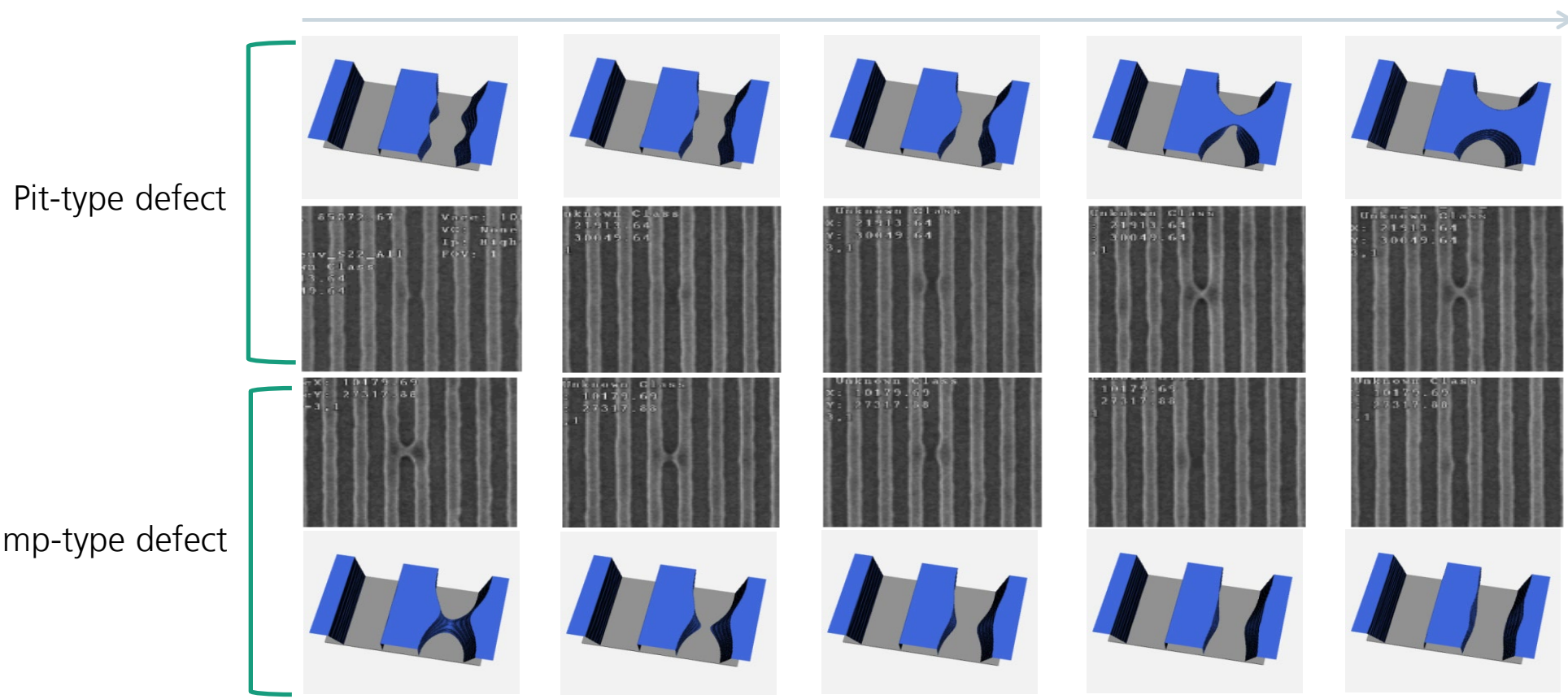
Steps Used in the Front-end-of-line of Chip Manufacturing

- These steps are carried out up to on-chip metallization
- TCAD allows one to study the impact of process variations on the behavior of the manufactured devices



Simulation of Lithography

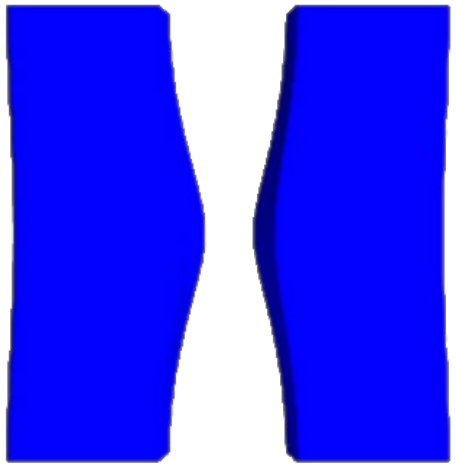
- Printing analysis of EUV multilayer mask defects for 40 nm lines and spaces, simulations with Dr.LiTHO of Fraunhofer IISB



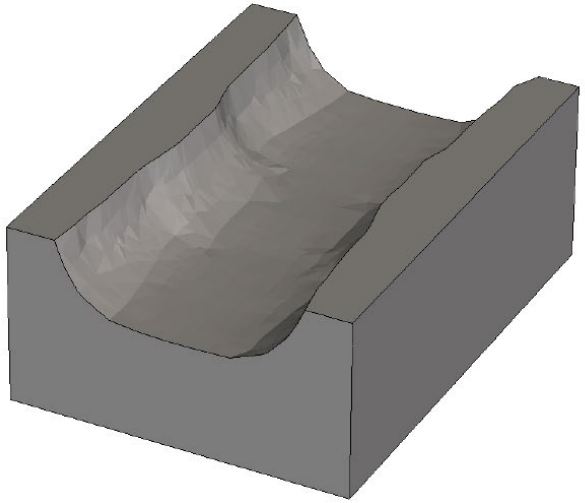
Simulation of Etching

- Using the simulated resist as masking layer, etching simulation with the IISB tool ANETCH predicts the shape of the etched structure

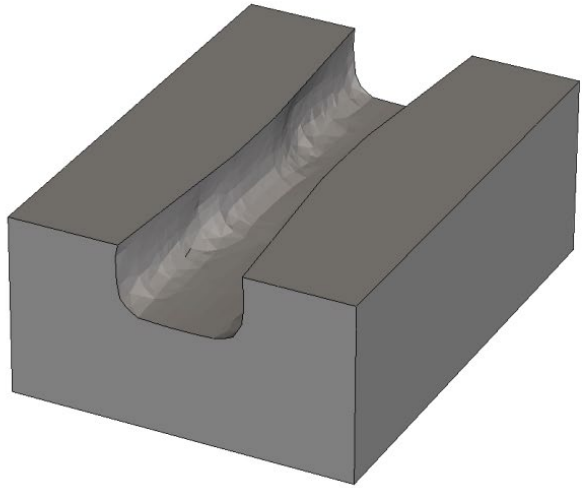
- In the example, the transfer of a resist pattern to the underlying layer is shown for isotropic and anisotropic etching (for better visualization, the resist mask is not shown for the etched structures)



Simulated resist mask



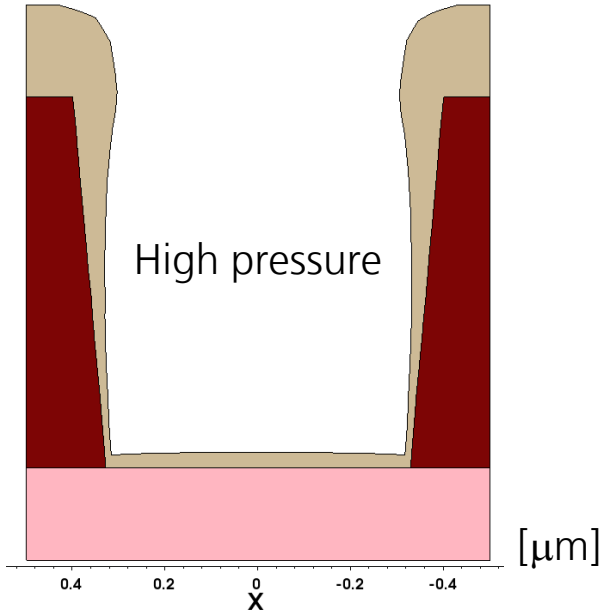
Isotropic etching

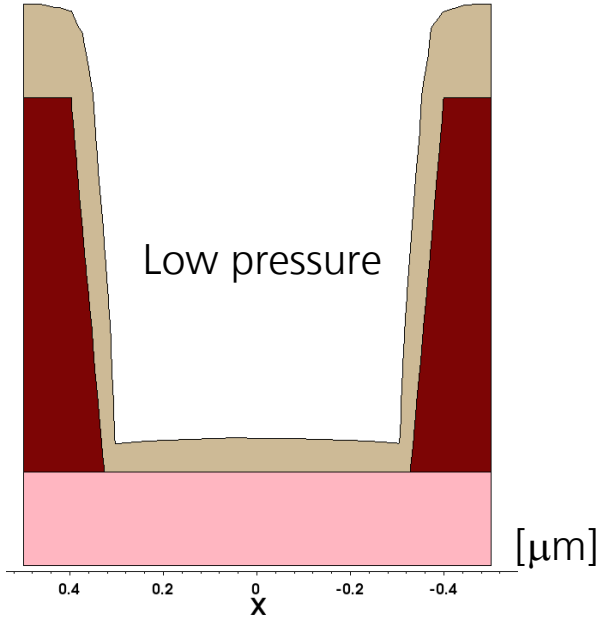


Anisotropic etching

Simulation of Conventional Sputter Deposition

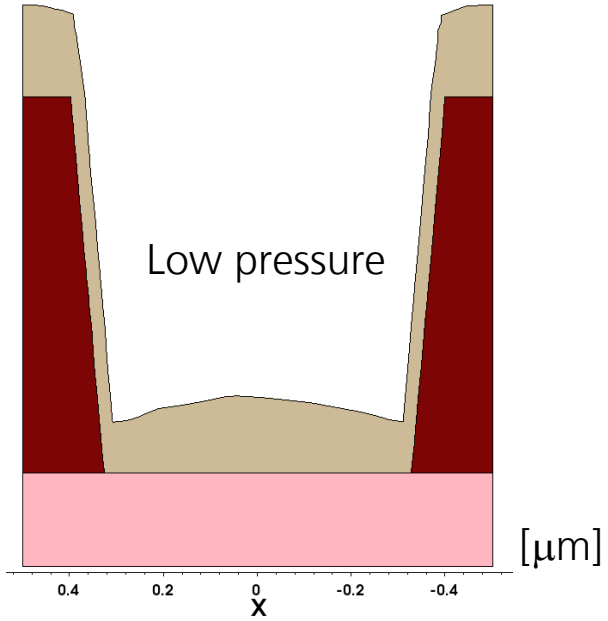
- Sputter deposition at high pressure and at low pressure (target diameter = 200 mm)





Distance target – substrate

= 100 mm



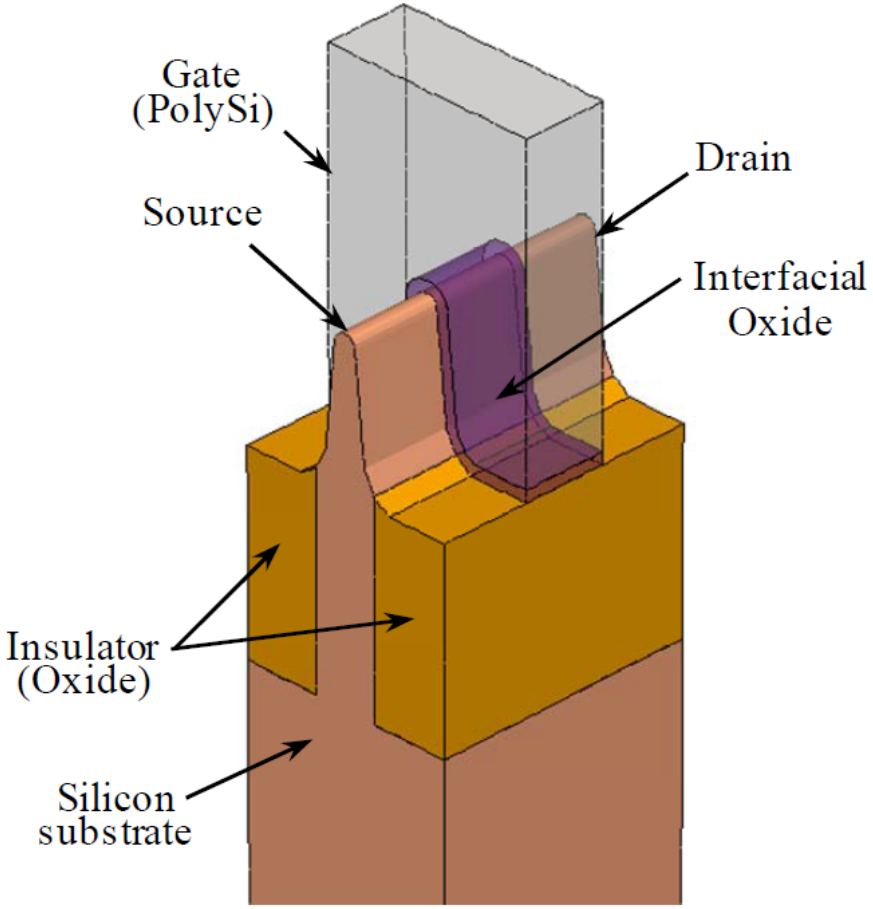
Distance target – substrate

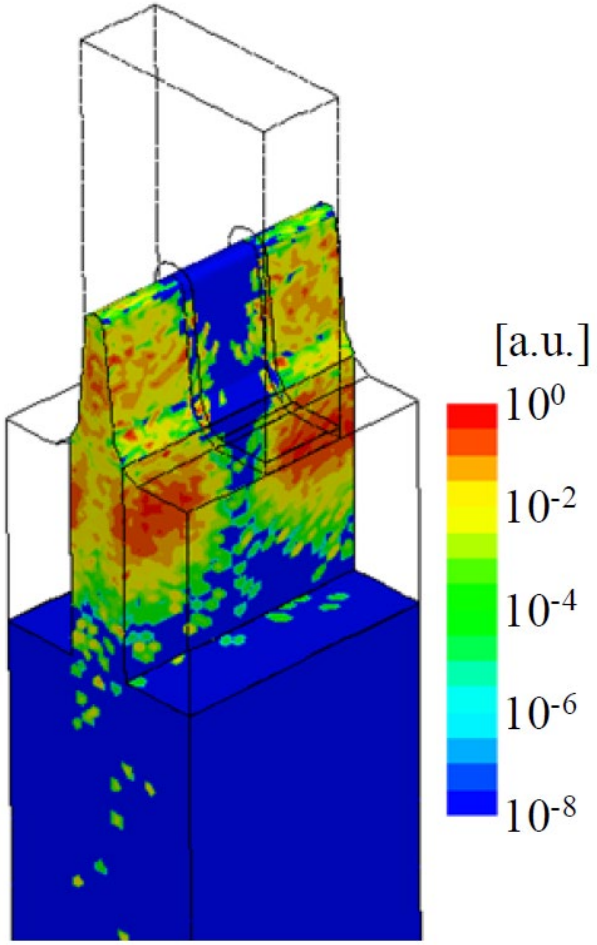
= 200 mm

Simulation of Ion Implantation

- 3D simulation of implantation of arsenic into a FinFET structure using the trajectory splitting method
- Figure shows the as-implanted concentration

  Energy = 20 keV
  Dose = $2 \cdot 10^{14}$ cm^{-2}





From Kubotera et al., Proc. IIT 2014

Simulation of a Fully-depleted Silicon-on-insulator Transistor

Data

Simulation modules

Equipment settings (geometry, pressure, mass flows, bias voltage, inductive power) of ICP reactor (Cl plasma)

Equipment simulation of ICP reactor

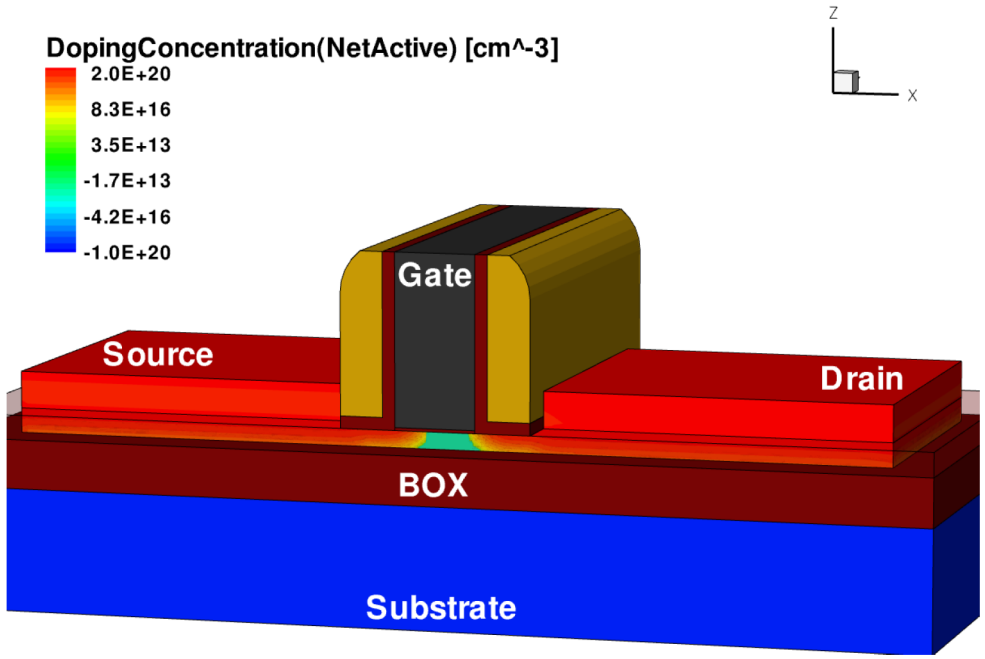
Ion fluxes (incl. angular characteristics) and neutral fluxes across wafer

Feature-scale simulation to determine gate profiles and CD (critical dimension) values

Gate CD probability distribution

SPICE compact modeling of transistors and SRAM cells

Probability distribution of electrical parameters



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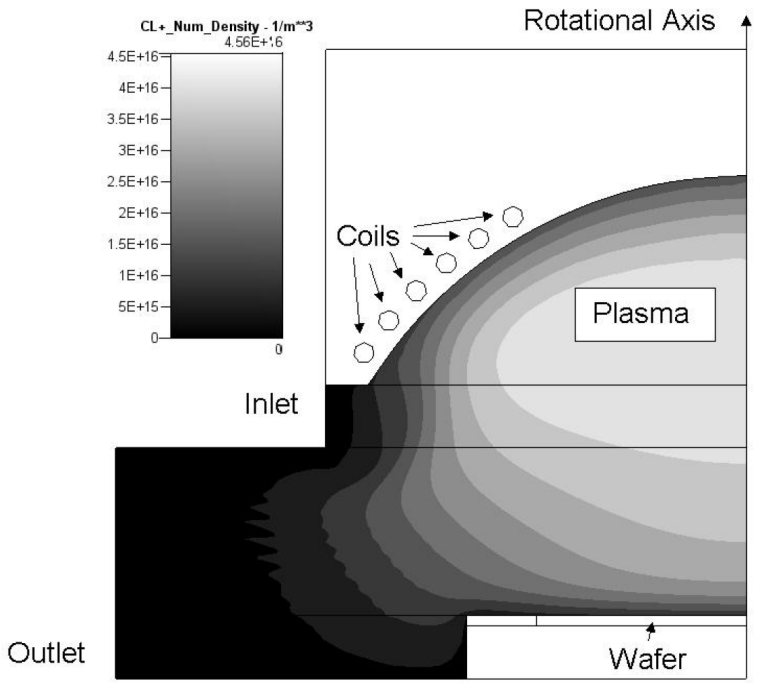
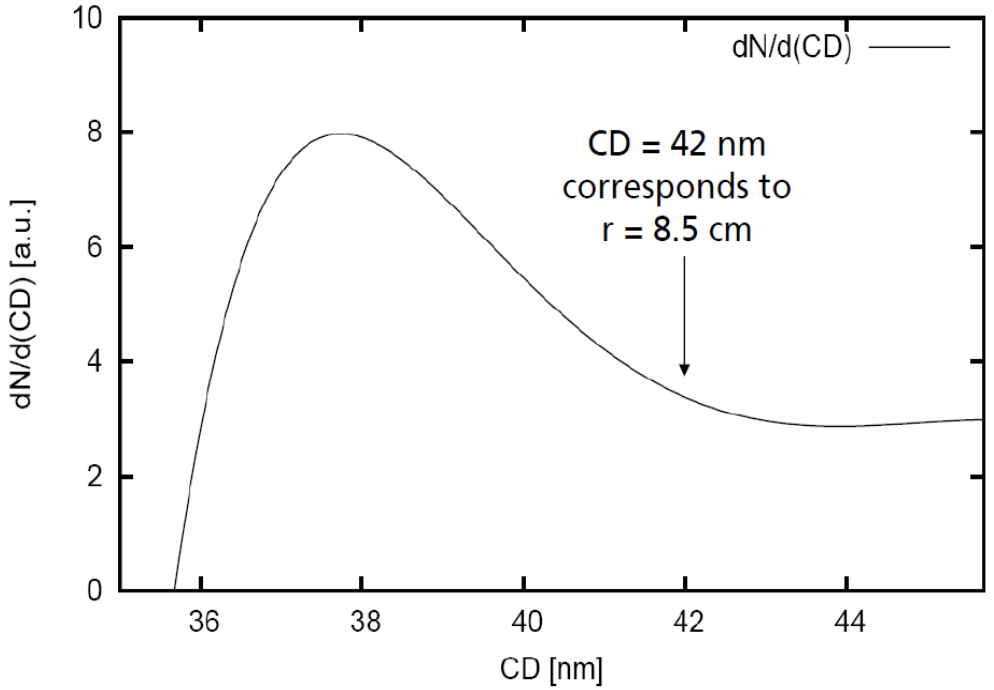
Simulation of a Fully-depleted Silicon-on-insulator Transistor

- Plasma equipment simulation (tool ESI-CFD) provides the fluxes of radicals and ions and its variation across the wafer (left figure shows the Cl ions as example)
- Coupled feature-scale simulation of gate patterning with the IISB tool ANETCH provides the corresponding CD values which can be transformed into a frequency distribution (right figure)





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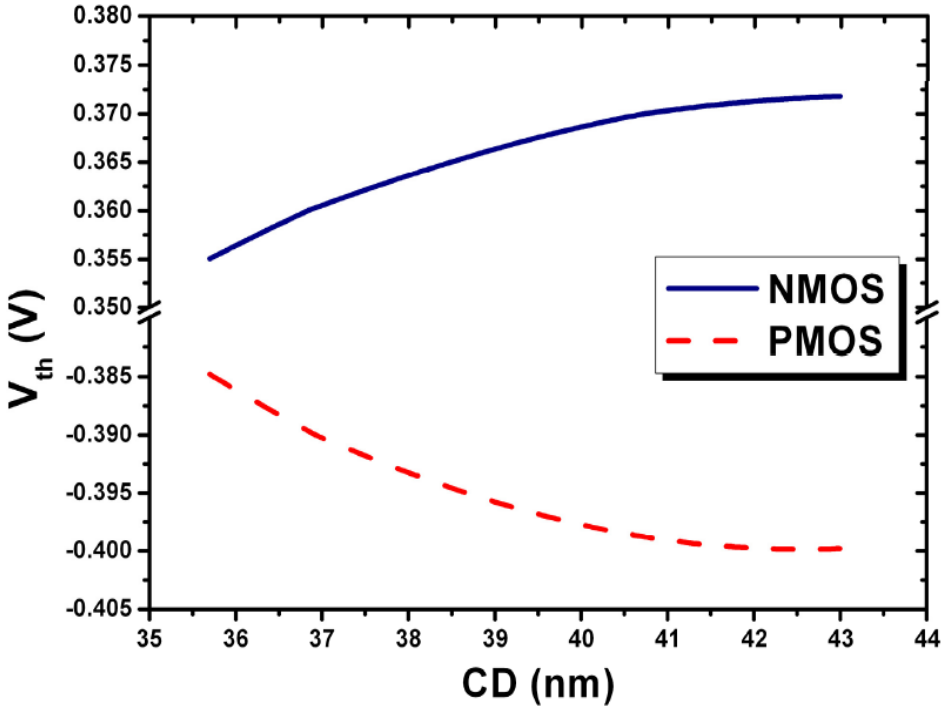
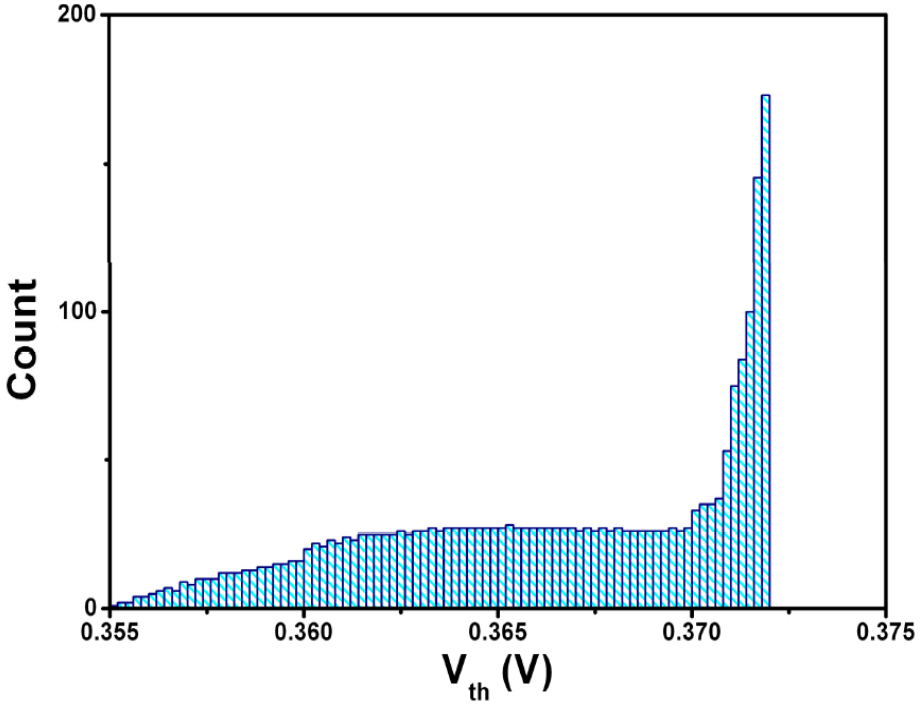
Simulation of a Fully-depleted Silicon-on-insulator Transistor

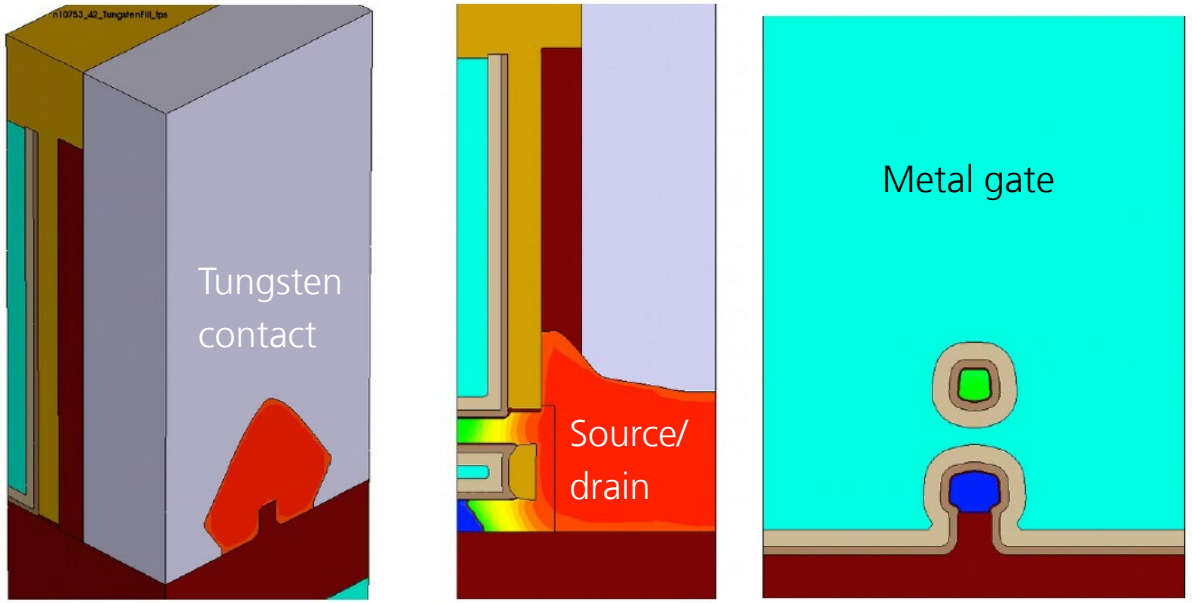
- Device simulation (Synopsys Sentaurus) provides the relation between CD and threshold voltage (left figure)
- Using the frequency distribution of the CD values then allows one to determine the probability distribution of the threshold voltage (right figure shown for NMOS)





Process Simulation of a Stacked Nanowire Field Effect Transistor (NW-FET)

- The structure consists of two silicon nanowires fabricated out of a silicon-on-insulator (SOI) substrate
- Width of the nanowires ≈ 10 nm
- The gate electrode is fabricated as a high-k metal-gate stack
- The source and drain regions have been fabricated by epitaxy, leading to the faceted raised source/drain contacts

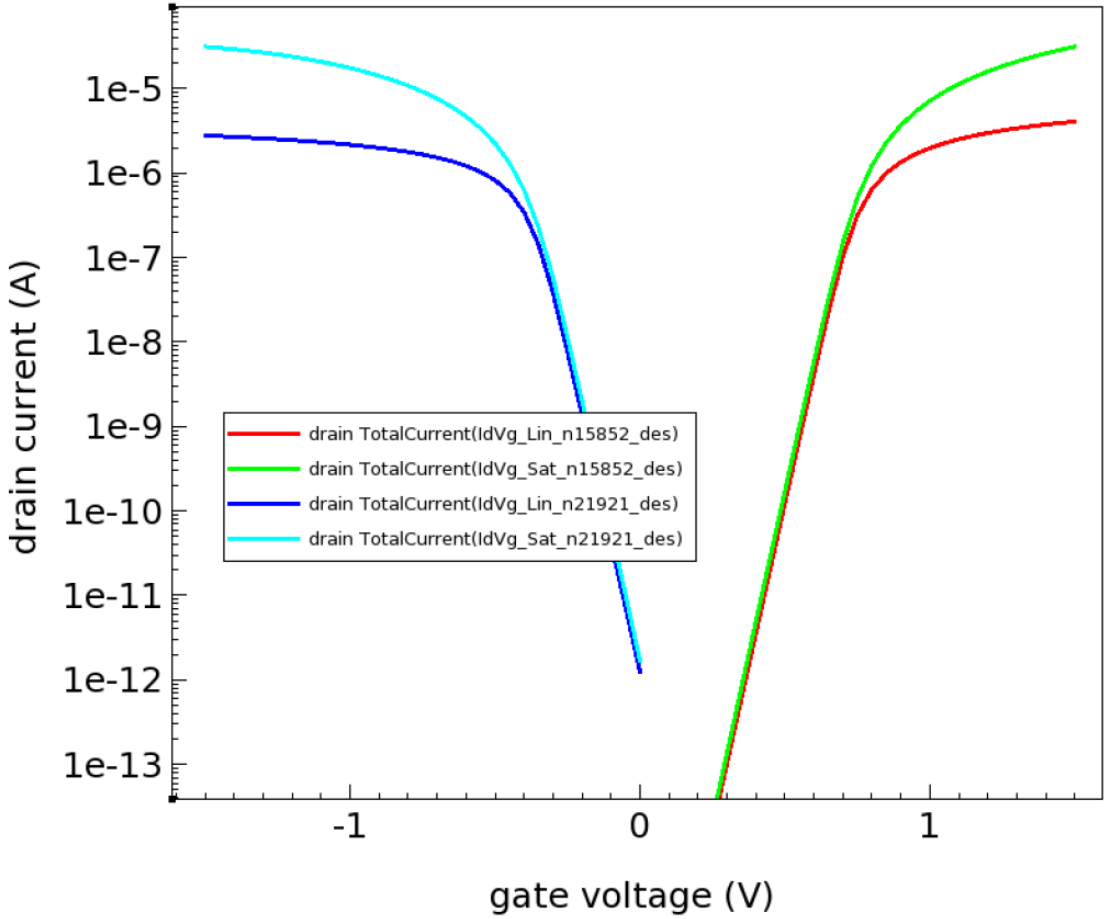


NW-FET structure after fabrication of gate electrode and tungsten plug as device contact in 3D view (left) and cross sections along and vertical to the wires (middle and right)

Simulations were carried out with Synopsys Sentaurus

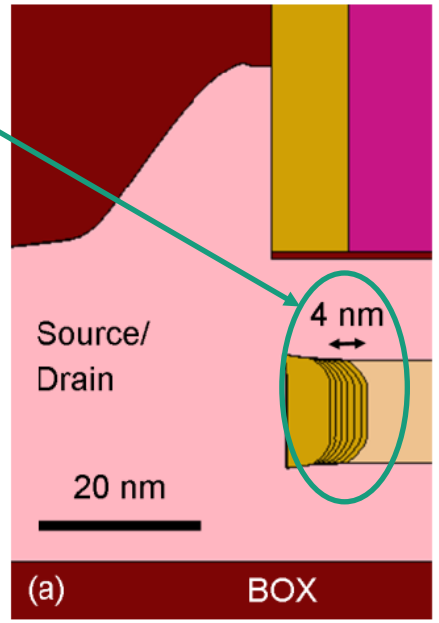
Device Simulation of a Stacked Nanowire Field Effect Transistor

- Extraction of the electrical characteristics
- Example shows simulated static transfer characteristics for NMOS transistor (curves on the right side) and PMOS transistor (curves on the left side)
- The curves are shown for source drain voltages in the linear and in the saturation regime

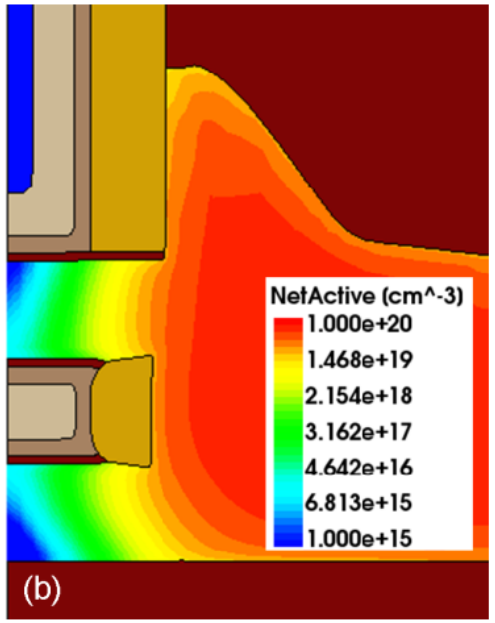


Variation of Stacked Nanowire Field Effect Transistor Performance (1)

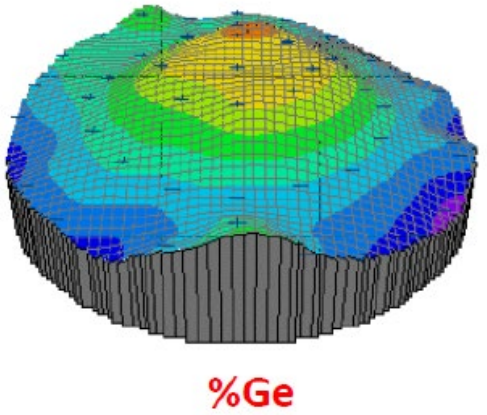
- Variations for the inner spacers are due to the variations of the germanium content x_{Ge} of the Si-Ge sacrificial layer used within the process flow
- Influence of these variations on the device behavior has been studied by means of numerical simulations



After S/D epitaxy

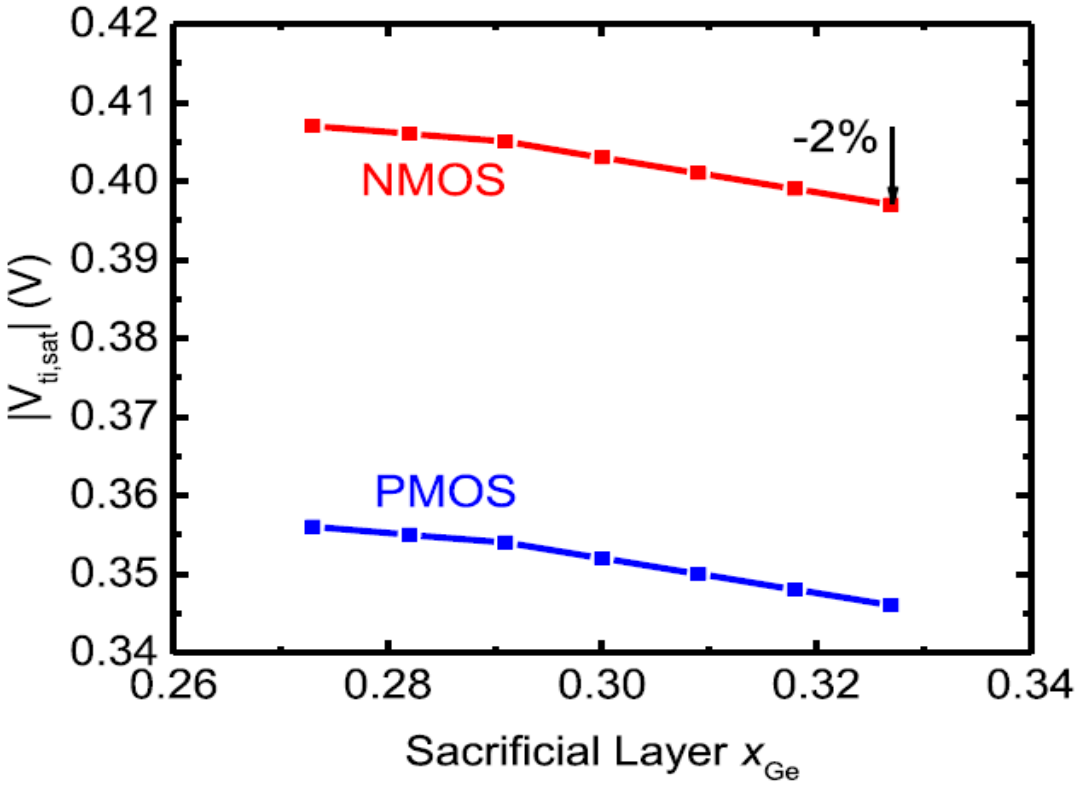


After gate stack deposition



Across-wafer distribution of germanium content

Variation of Stacked Nanowire Field Effect Transistor Performance (2)

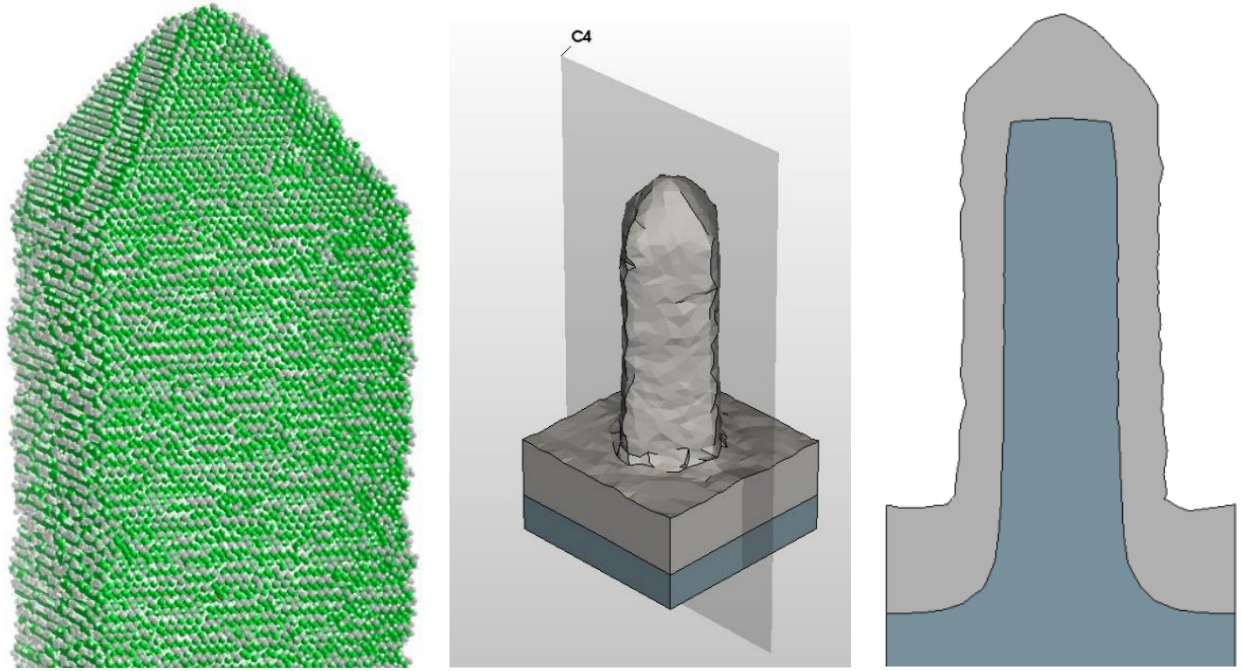


Dependence of the threshold voltage on the germanium content x_{Ge} of the sacrificial layer

Future Perspectives

Simulation of Advanced Nanostructures (1)

- Example: atomistic process simulation of chemical vapor deposition (CVD) on a nanowire structure
- Appropriate interfaces are needed to feed these results into the simulation of the complete process flows
- Such interfaces have been developed within the project MUNDFAB (Modeling Unconventional Nanoscaled Device FABrication), www.mundfab.eu
- Left: atomistic simulation with the tool MulSKIPS from CNR-IMM, Catania, of Si CVD growth with SiH_2Cl_2, HCl and H_2 precursors, the deposited layer shows faceting
- Right: structure converted to a continuum description based on entities given as polyhedrons



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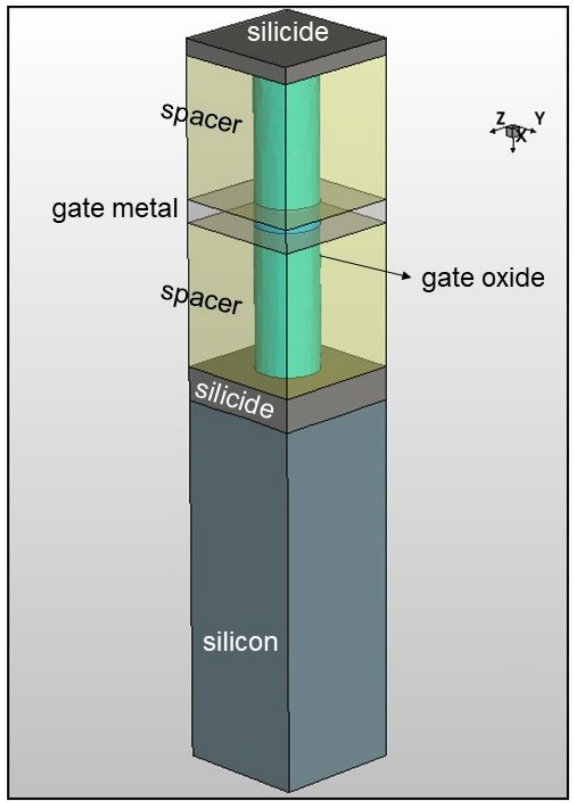
Simulation of Advanced Nanostructures (2)

- 3D process and device simulations of vertical junctionless Gate-all-around nanowire FETs (Synopsys Sentaurus)
- Thinning of the nanowires to the desired diameter is obtained by sacrificial wet oxidation, followed by dry oxidation to grow the gate oxide
- The silicidation steps has been simulated with MulSKIPS, interfacing with the simulation of the other process steps has been carried out with MUNDFAB tools



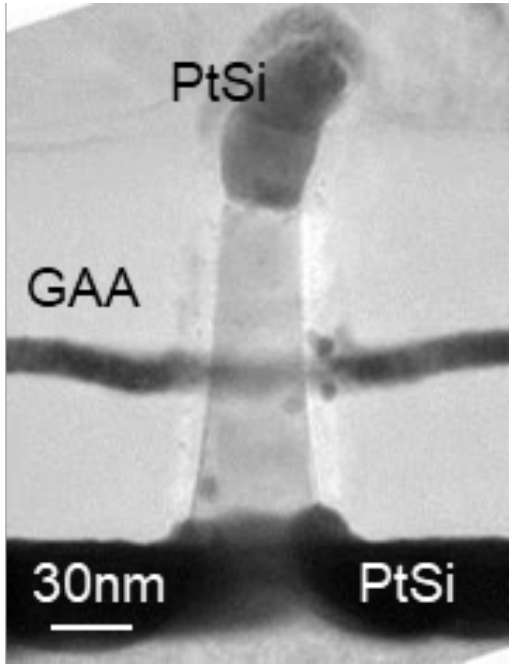
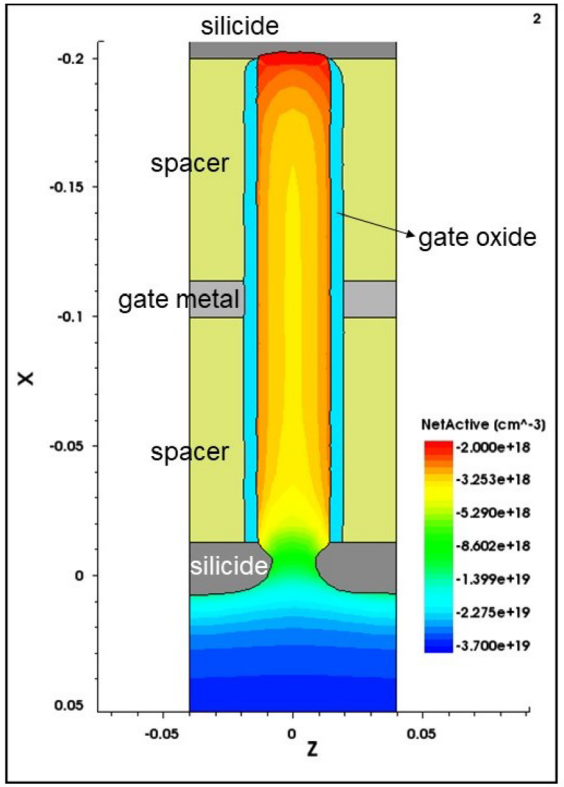
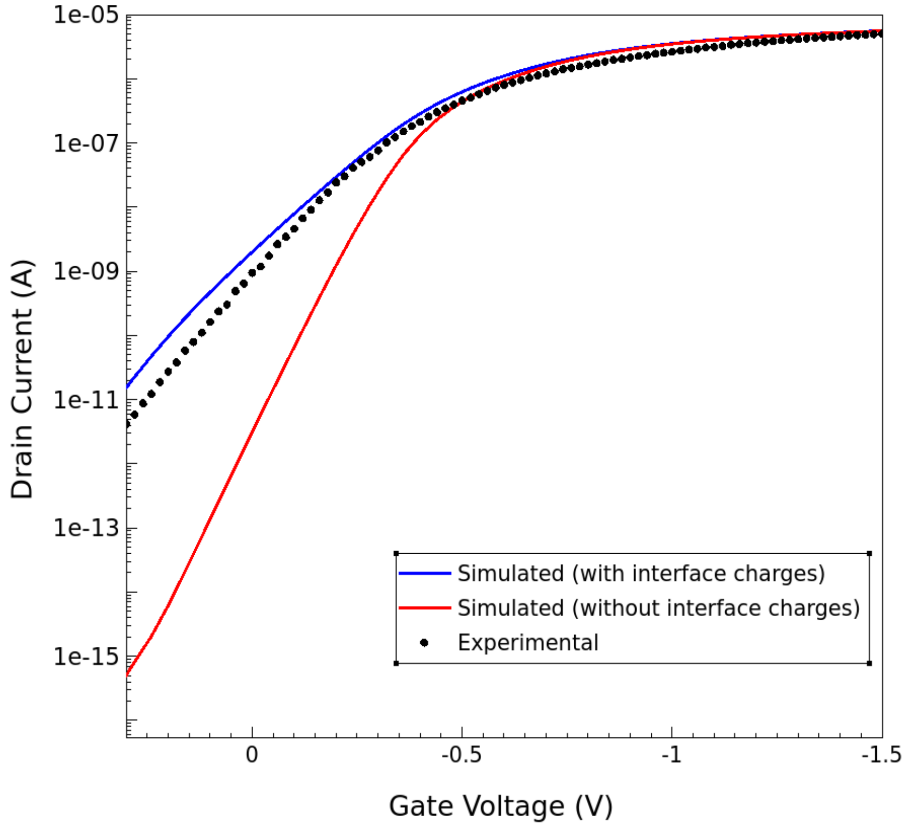


Figure: Larrieu et al., Nanoscale, 2013

Simulation of Advanced Nanostructures (3)

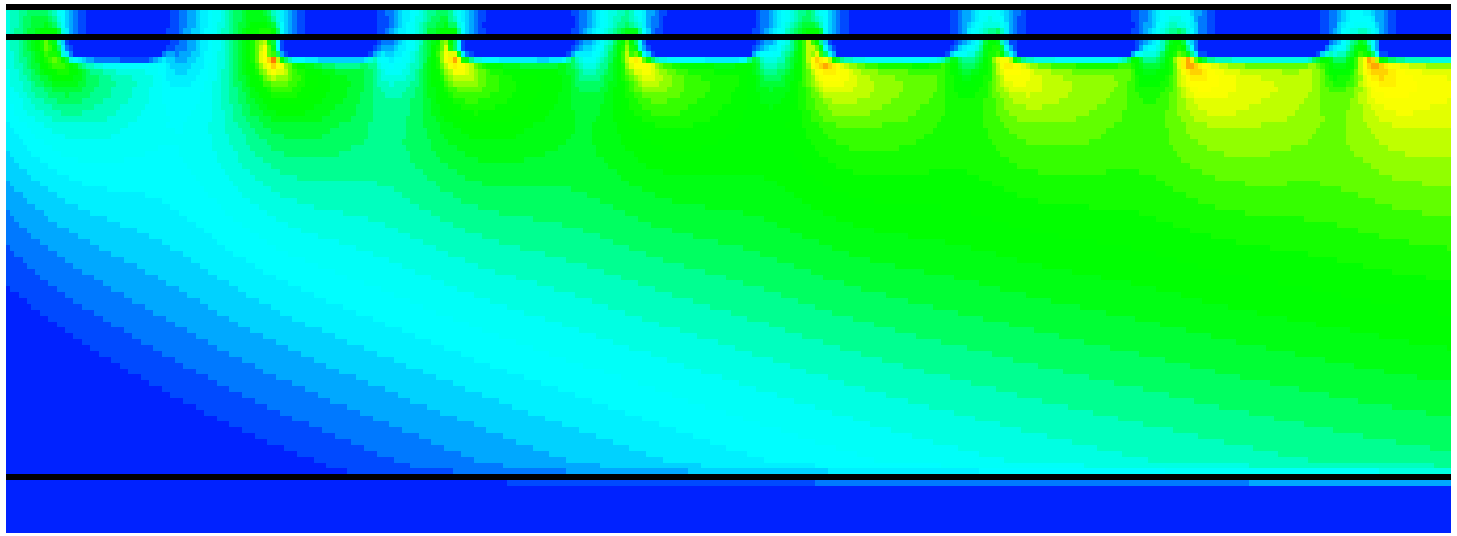
- Doping concentration computed using the ChargedPair diffusion model and the three-phase segregation model4 with the parameter set from Sentaurus AdvancedCalibration U-2022.12
- In the device simulation, the influence of fixed charges at the interface between silicon and silicon oxide is considered
- For the transfer characteristics, including the interface charges leads to better agreement between simulation and measured data





TCAD Tool Development and Application

- For future work and projects, particularly the following is on our agenda:
  - Model and tool development for devices based on silicon carbide (SiC) and other wide-bandgap materials
  - TCAD extensions and applications for quantum computing and sensing



Simulated distribution of the electric field for a guard ring structure used for SiC high-voltage devices

Conclusions

- By combining process and device simulation, TCAD allows one to study process sequences and to investigate the impact of the manufacturing process and its parameters on the device characteristics
  - Process parameters can be tuned to obtain devices with the desired behavior
  - Variations of the processes can be mapped onto variations of the device characteristics
- For simulating the manufacturing of advanced devices, sophisticated physical and chemical models for the evolution of geometry and doping are required
- Besides the capabilities of the models, software integration and interfaces between different simulation tools are needed for running full process sequences in a chain up to device simulation
- At the IISB, commercial software tools are used in combination with inhouse and third-party simulation modules
- Future work will particularly focus on wide-bandgap devices and TCAD for quantum computing and sensing

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